INTERFACING WITH 8259 :→

* Programmable Interrupt Controller
* Manages 8 levels of interrupts (can be configured as Master Slave & cascade to handle 64 Interrupts.)
* Provides starting address of ISR
* Various Priority Modes :-
  a) Fixed Priority
  b) Automatic Rotating Priority
  c) Specific Priority

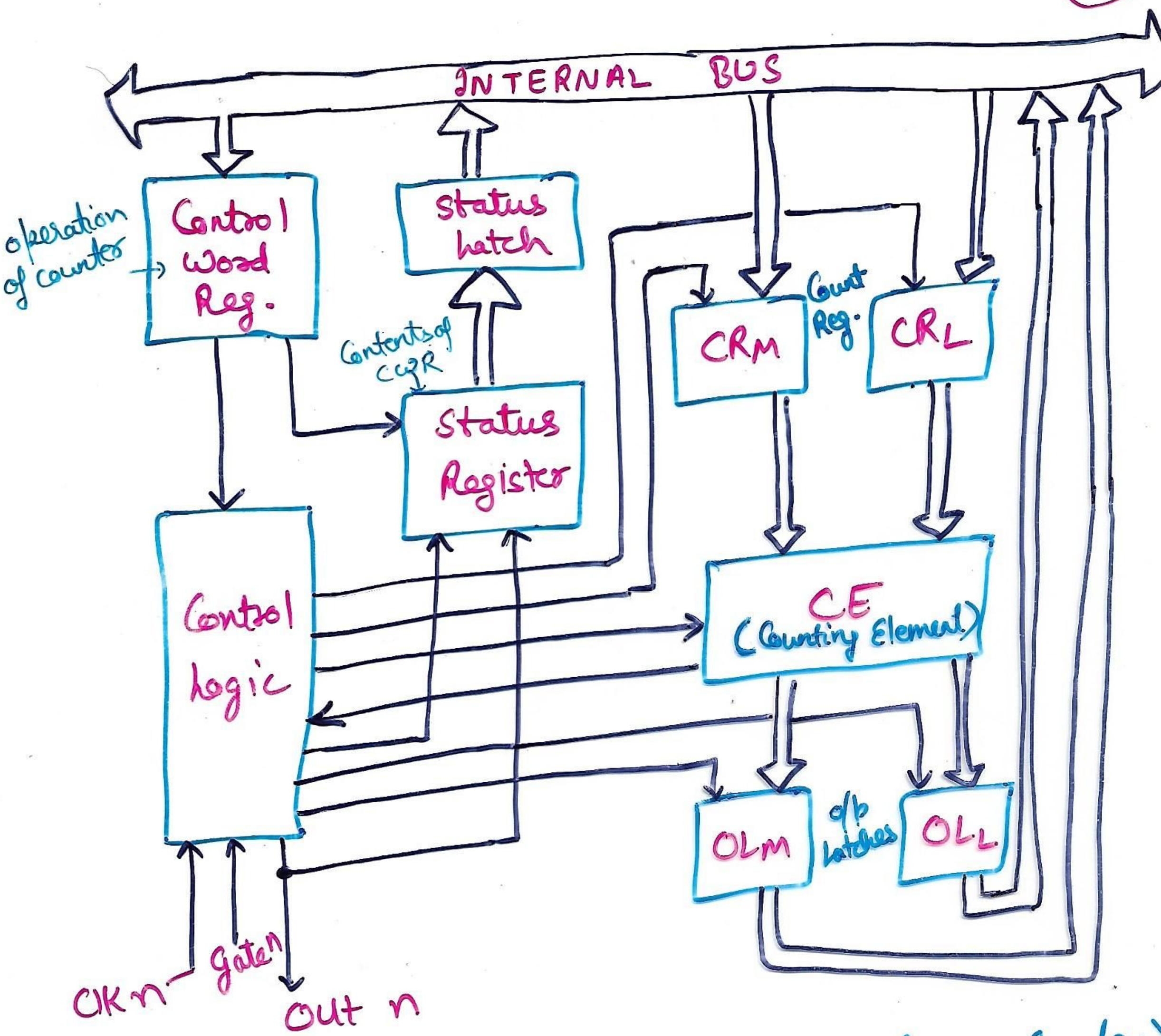
→ Funnel interrupt signals on a single interrupt i/p, INTR (of NMI is reserved for power failure.

IMR :→ To disable (mask) or enable (unmask) individual intr. signals.
↳ Unmasked by sending 0 with a command word in part. bit position

IRR :→ Bit set acc. to Intr. Requests (More than one can be set)

ISR :→ Bit set acc. to Serviced Intr. (currently)

PR :→ Judges the servicing codes



* CE C Presettable Synchronous Down Counter
* OL follows the CE
* CR to load new count into Register
* CL allows one Register at a time to be loaded from Internal Bus
* CE cannot be written into, Count is always written to CR.

Control Word Format :⇒

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC_1	SC_0	RL_1 / RW_1	RL_0 / RW_0	M_2	M_1	M_0	BCD

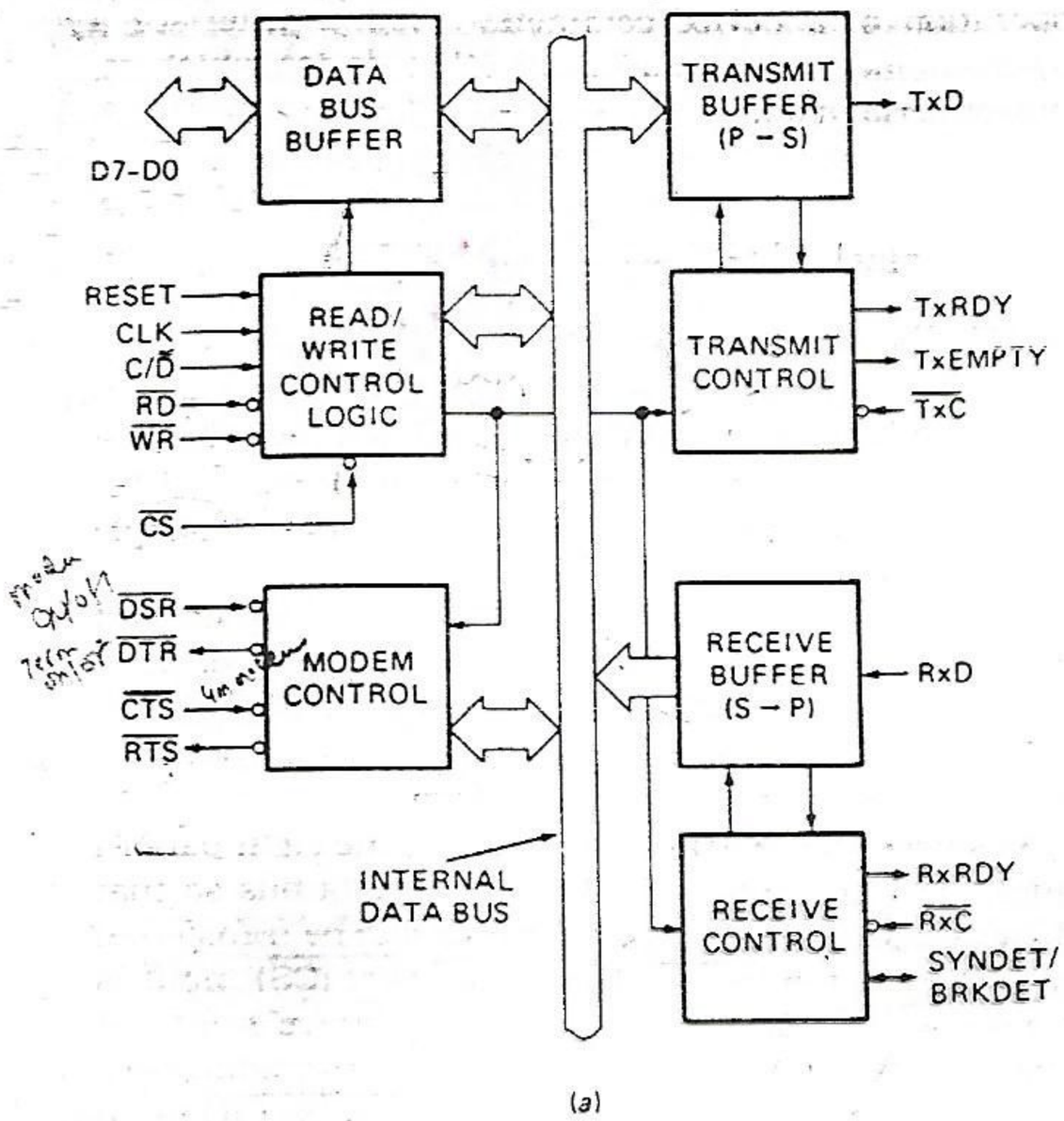
BCD: 1 → BCD, 4 Decades
Binary: 0 → Binary, 16 bits

SC_1	SC_0	Select
0	0	Counter 0
0	1	C_1
1	0	C_2
1	1	Read back

RL_1	RL_0	Operation
		Counter latch
0	0	R/W LSB only
0	1	R/W MSB only
1	0	R/W LSB first & then MSB
1	1	

M_2	M_1	M_0	Mode
0	0	0	Mode 0 (Intr on Terminal Count)
0	0	1	M_1 (H/W Retriggerable one shot)
X	1	0	M_2 (Periodic Int. Timer)
X	1	1	M_3 (Square Wave Gen.)
1	0	0	M_4 (S/W Triggered Strobe)
1	0	1	M_5 (H/W Triggered Strobe Retriggerable)

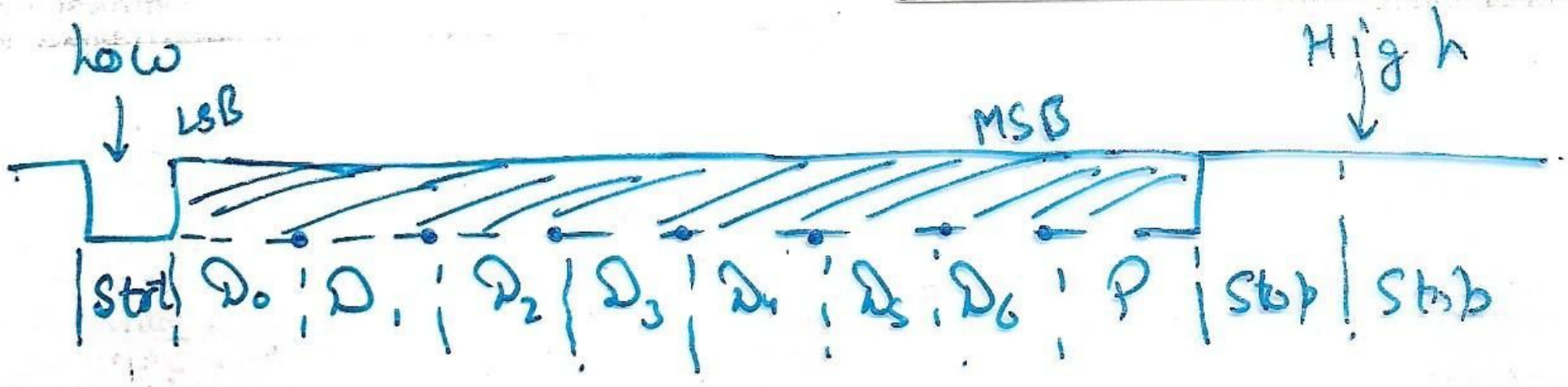
8251



(a)

8251 Pin Functions

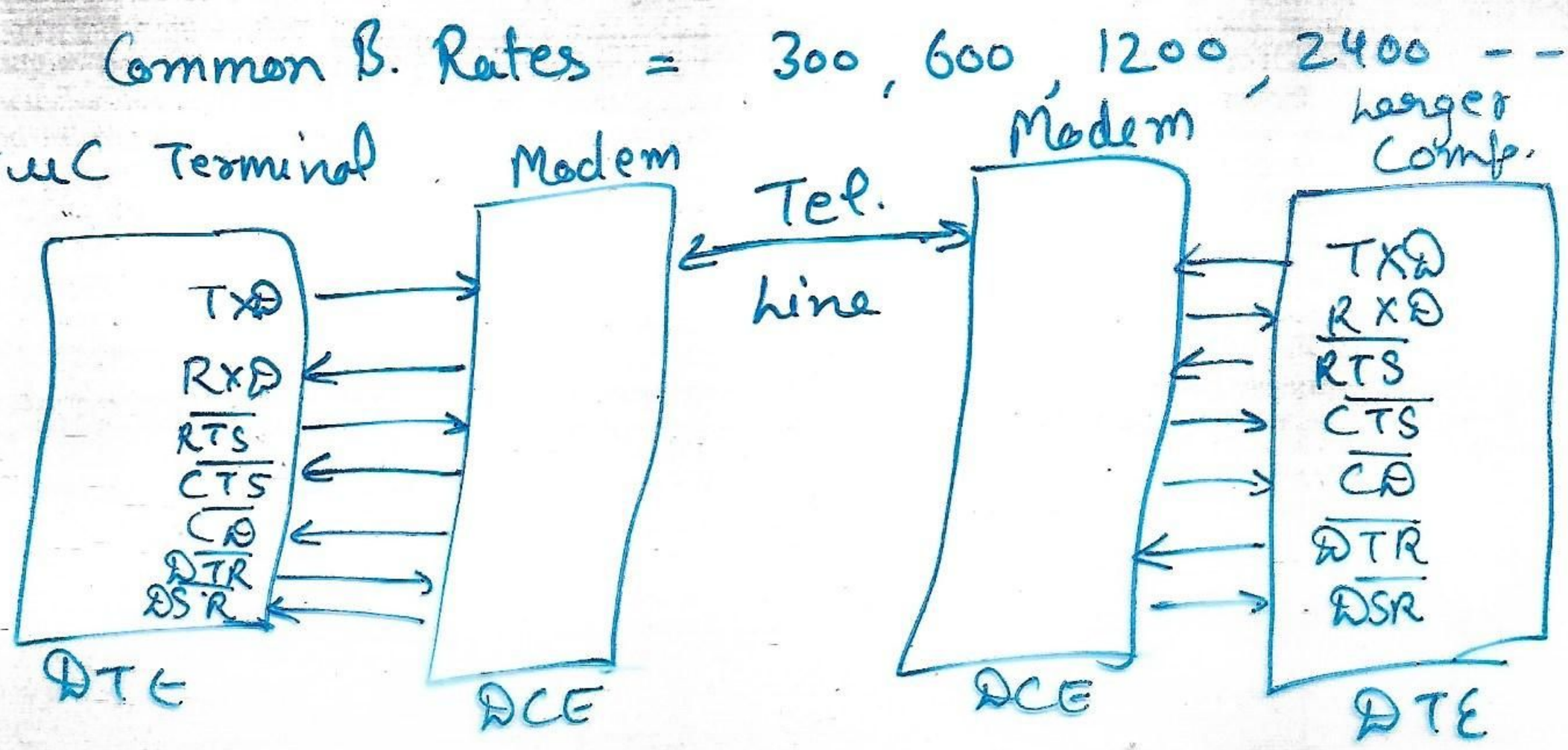
Pin Name	Pin Function
D7-D0	Data bus (8 bits)
C/$\overline{D}$	Control or data is to be written or read
$\overline{RD}$	Read data command
$\overline{WR}$	Write data or control command
$\overline{CS}$	Chip select
CLK	Clock pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter clock
TxD	Transmitter data
$\overline{RxC}$	Receiver clock
RxD	Receiver data
RxRDY	Receiver ready (has character for CPU)
TxRDY	Transmitter ready (ready for char. from CPU)
$\overline{DSR}$	Data set ready
$\overline{DTR}$	Data terminal ready
SYNDET/BD	Sync detect/break detect
$\overline{RTS}$	Request to send data
$\overline{CTS}$	Clear to send data
TxEMPTY	Transmitter empty
V_{cc}	+5-V supply
GND	Ground

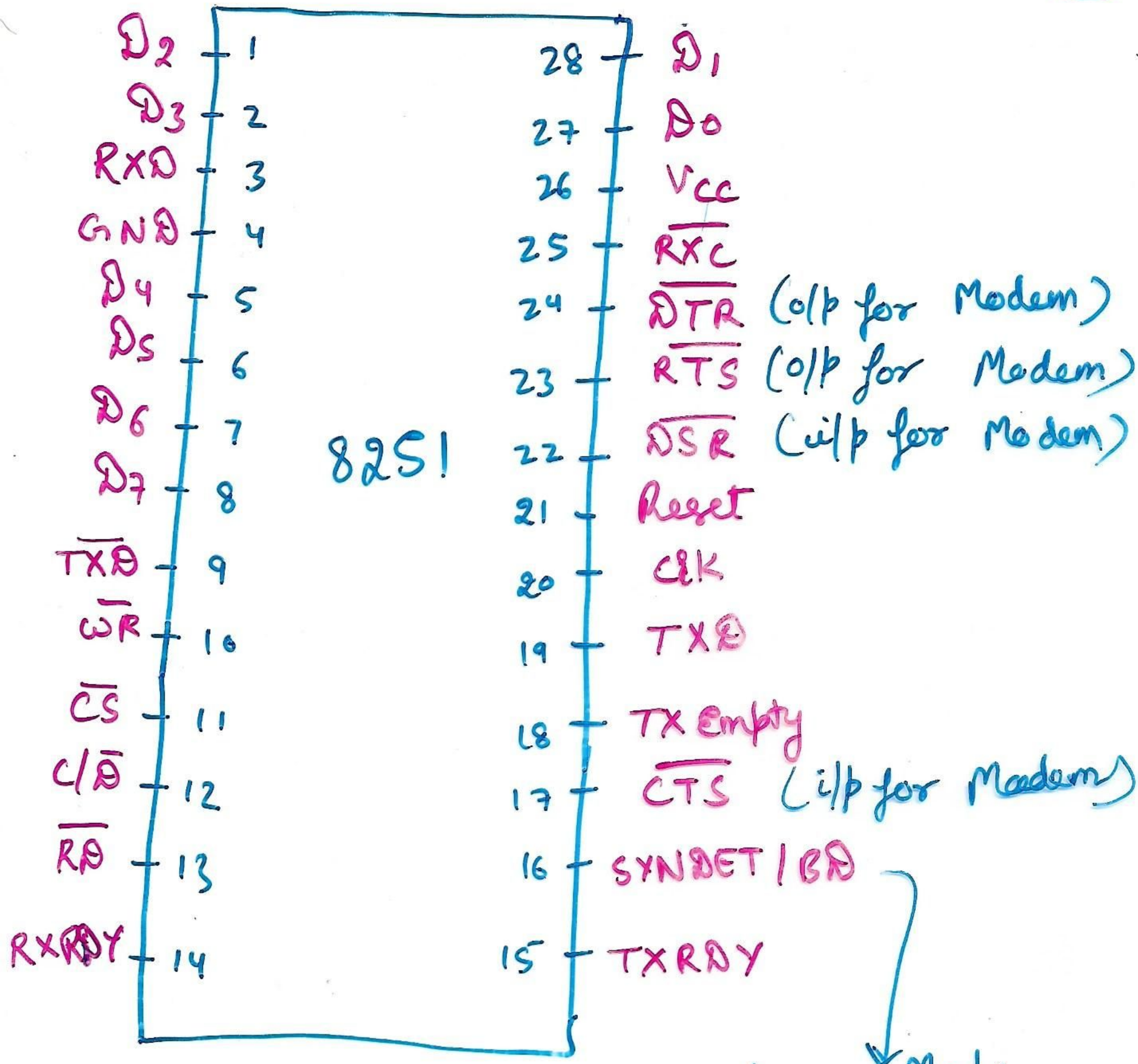


Bit format for Asynchronous Serial Data

Baud Rate = $\frac{1}{\text{Time b/w Signal Transitions}}$

Common B. Rates = 300, 600, 1200, 2400 --





* Function changes acc. to

1) Int. Sync → High
   status word → low

2) Ext. Syn →
   High for i/p terminal

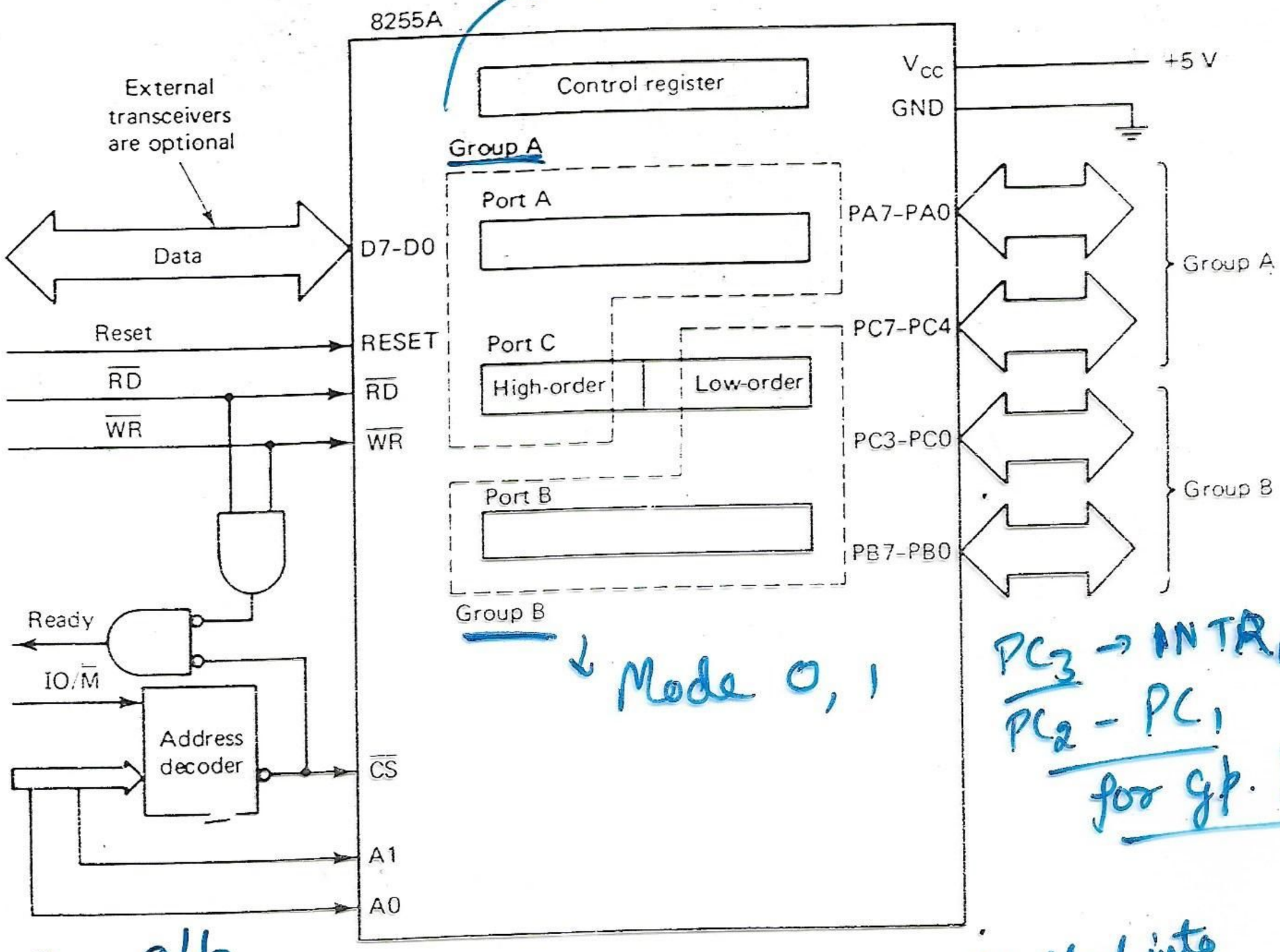
3) Asyn. → o/p terminal
   High for detection of Break char.
   low for RXD is high.

4A

8255

5

Mode 0, 1, 2



↓ Mode 0, 1

$PC_3 \rightarrow INTR_A$
$PC_2 - PC_1$ for gp. B

0 → o/p
1 → i/p

Figure 9-21 Diagram of the 8255A.

(Divided into 2 sets)

D_4 — Port A
D_3 — Port C 'MSB'
D_1 — Port B
D_0 — Port C 'LSB'

Mode 0

Each set may be used for i/p | o/p, but not both

Port C → Handshaking & control signals

PC_4 — $\overline{STB_A}$ → P_0-P_7 latched in port A
PC_5 — IBF (i/p buffer full)
PC_6 — PC_7 — $\overline{ACK}$ — $\overline{OBF}$
Status/Ctrl. signals
~~accept~~ data from port A

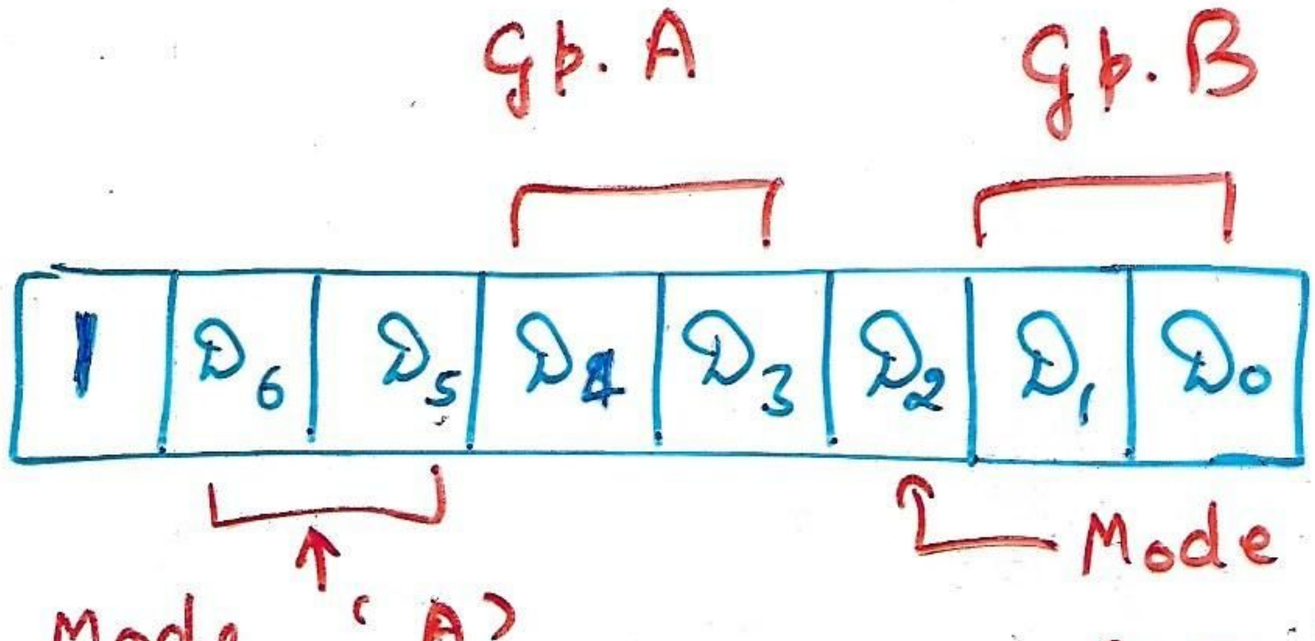
Mode 1

gp. A → Port A for i/o acc. to D_4

4C

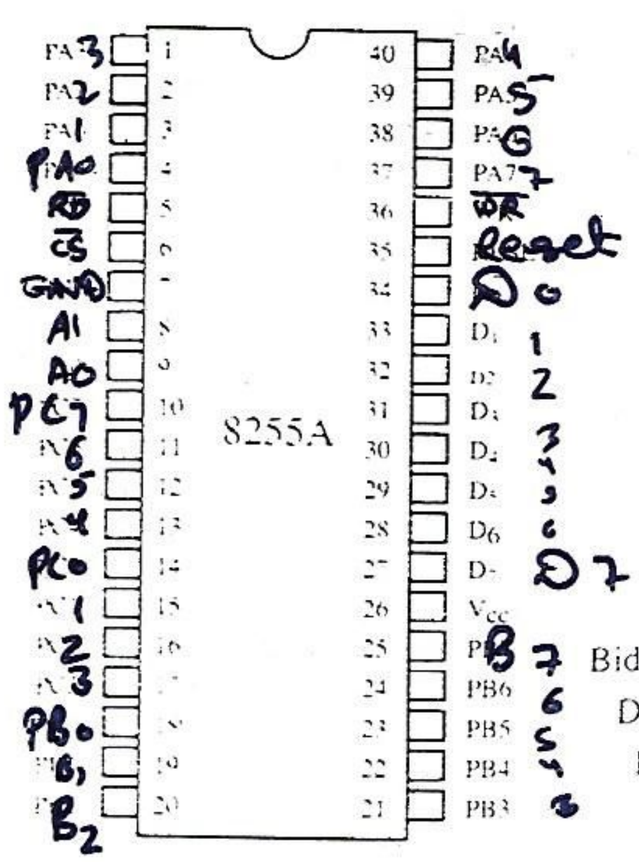
Table 8–4.
Truth Table for the 8255A PPI (Courtesy of Intel Corporation.)

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
					Input operation (READ)
0	0	0	1	0	Port A → data bus
0	1	0	1	0	Port B → data bus
1	0	0	1	0	Port C → data bus
					Output operation (WRITE)
0	0	1	0	0	Data bus → port A
0	1	1	0	0	Data bus → port B
1	0	1	0	0	Data bus → port C
1	1	1	0	0	Data bus → control
					Disable function
X	X	X	X	1	Data bus tristate
1	1	0	1	0	Illegal condition
X	X	1	1	0	Data bus tristate



8255 Control Register

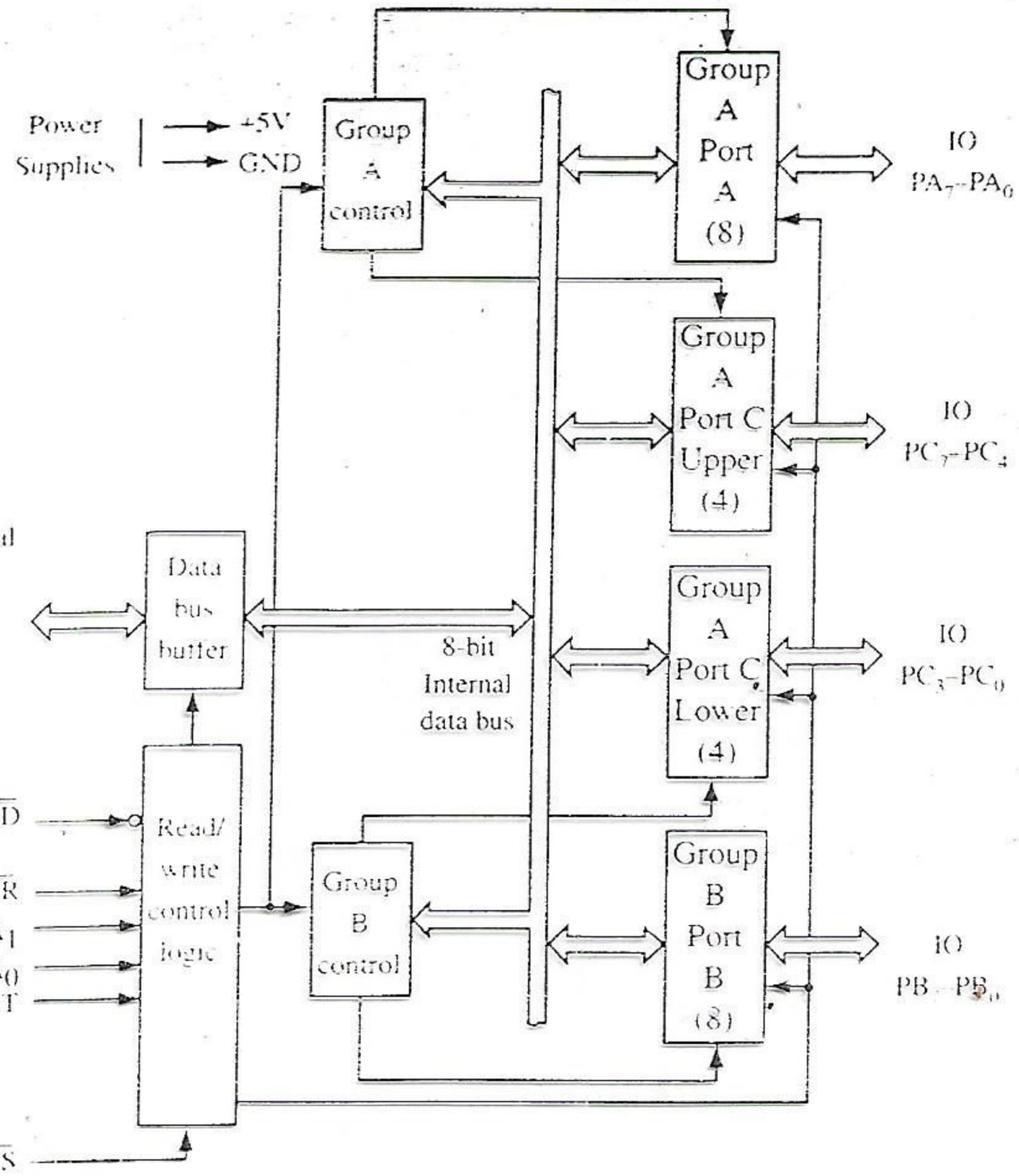
Pin Configuration



Pin Names

D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7–PA_0	Port A (bit)
PB_7–PB_0	Port B (bit)
PC_7–PC_0	Port C (bit)
V_{cc}	+5V
GND	0V

8255 Block Diagram



Mode 2 : → Applies only to Gp. A

↳ Port A is Bidirectional

PC_3 → Interrupt Requests

PC_4 → $\overline{STB_A}$

PC_5 → IBF_A

PC_6 → $\overline{ACK}$ (Device ready to accept data from $PA_7 - PA_0$)

PC_7 → $\overline{OBF_A}$

↳ Gp. B can be in any mode

Interfacing with 8253/8254

* Software Programmable Timer/Counter

→ 8253/8254 each contain three 16-bit counters programmed to operate in different modes.

* Both are pin-to-pin compatible

① ↳ Maximum i/p Clock frequency

8253 → 2.6 MHz

8254 → 8-10 MHz

② ↳ Read back feature to allow to latch the count in all counters & status of counter at any point

8254 → ✓

8253 → X

↳ Parameters to be programmed are:-

a) Operation (BCD / Binary)

b) Count value

c) Mode Selection

d) Counter selection

App: → a) Real time Clock

b) Event Counter

c) Binary Rate Multiplier

d) Complex Motor Controller

e) Square Wave Generator etc

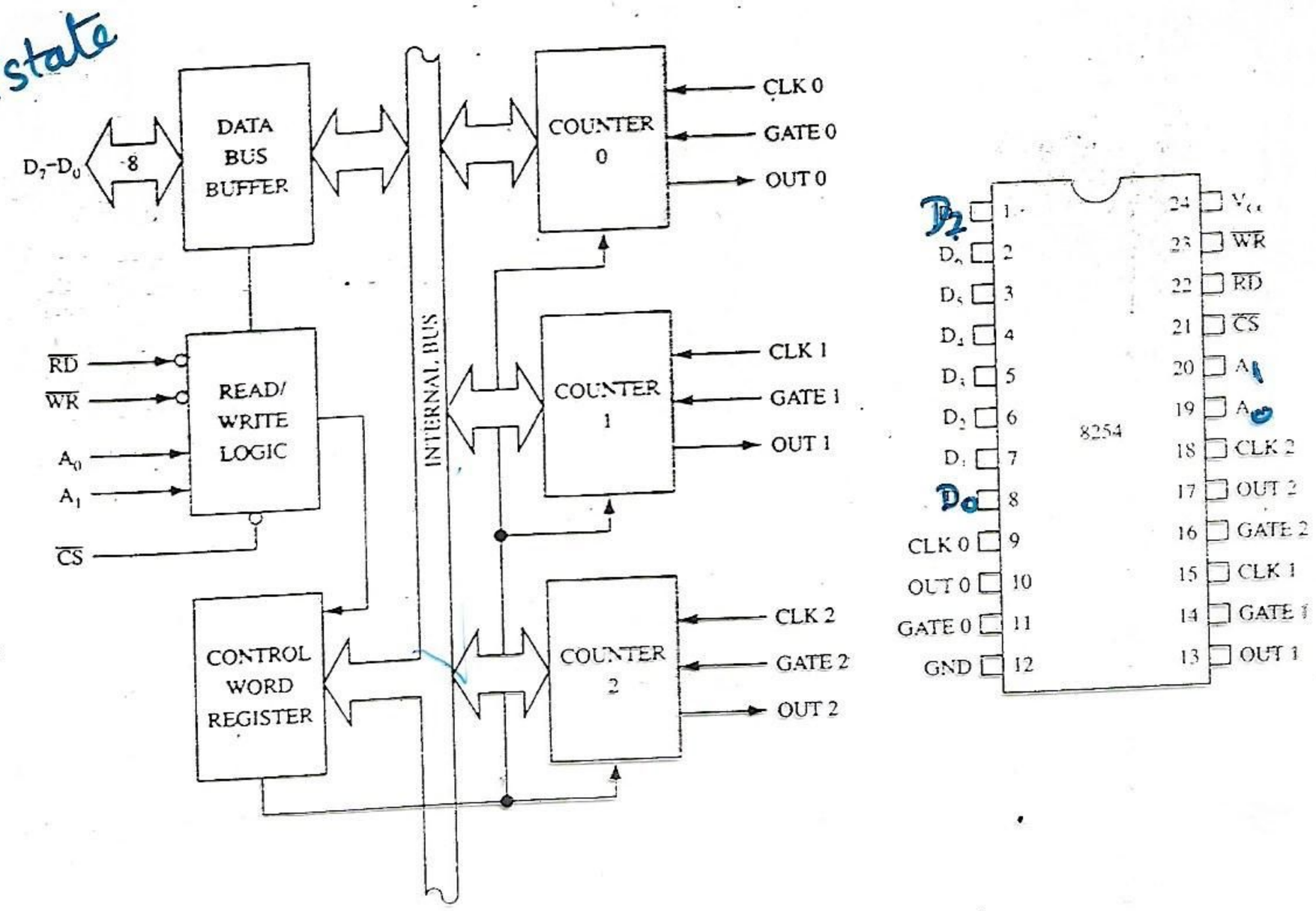


Figure 8–17.
Block diagram and pin descriptions for the 8254 programmable interval timer. Three separate timers/counters are provided.
(Courtesy of Intel Corporation.)

Table 8–6.
Possible I/O Operations

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Write into counter 0
0	1	0	0	1	Write into counter 1
0	1	0	1	0	Write into counter 2
0	1	0	1	1	Write control word
0	0	1	0	0	Read from counter 0
0	0	1	0	1	Read from counter 1
0	0	1	1	0	Read from counter 2
0	0	1	1	1	No-Operation (3-State)
0	0	1	X	X	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1			

(Courtesy of Intel Corp.)

A_1	A_0	Selection
0	0	Counter 0
0	1	C 1
1	0	C 2
1	1	Control word Register

INTERFACING :-

8255 :→ PPI (Programmable Peripheral Interface)

* It consists of i/o ports to connect peripherals to 8086.
* Used for parallel data transfer
* It consists of three separately addressable ports A, B & C and a control register.
* $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ as control signals
* A_1, A_0 → which of four Registers addressed
* Bits in port C are sometimes used as control bits

→ D_7 of Byte of Control. Reg. is examined

↳ 1 → Transfer to Cont. Reg.

0 → Set/Reset Instruction to port C.

$D_1 - D_3$ → No. of bit to be changed

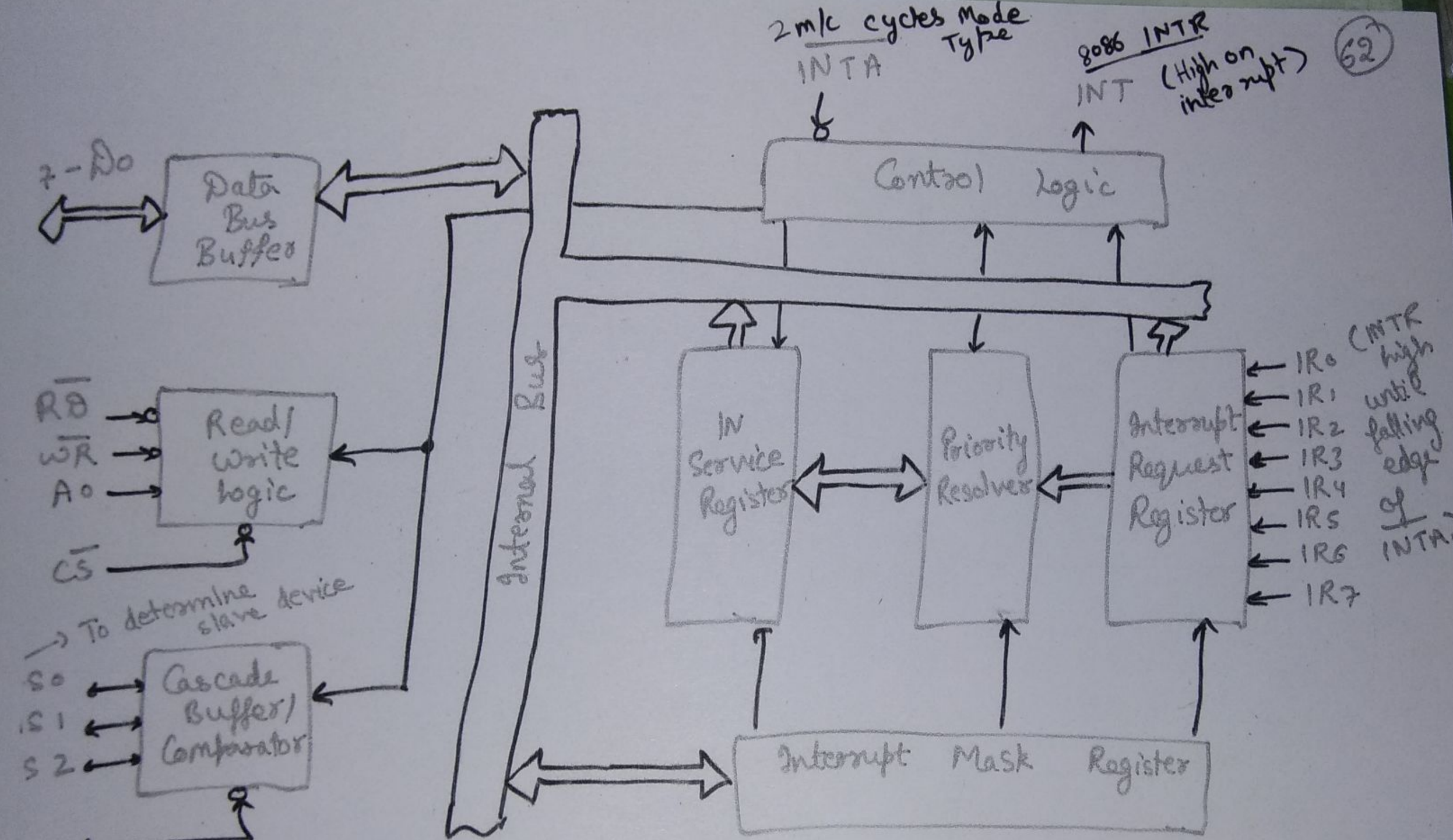
D_0 → To be set / clear

$D_4 - D_6$, Remaining are unused

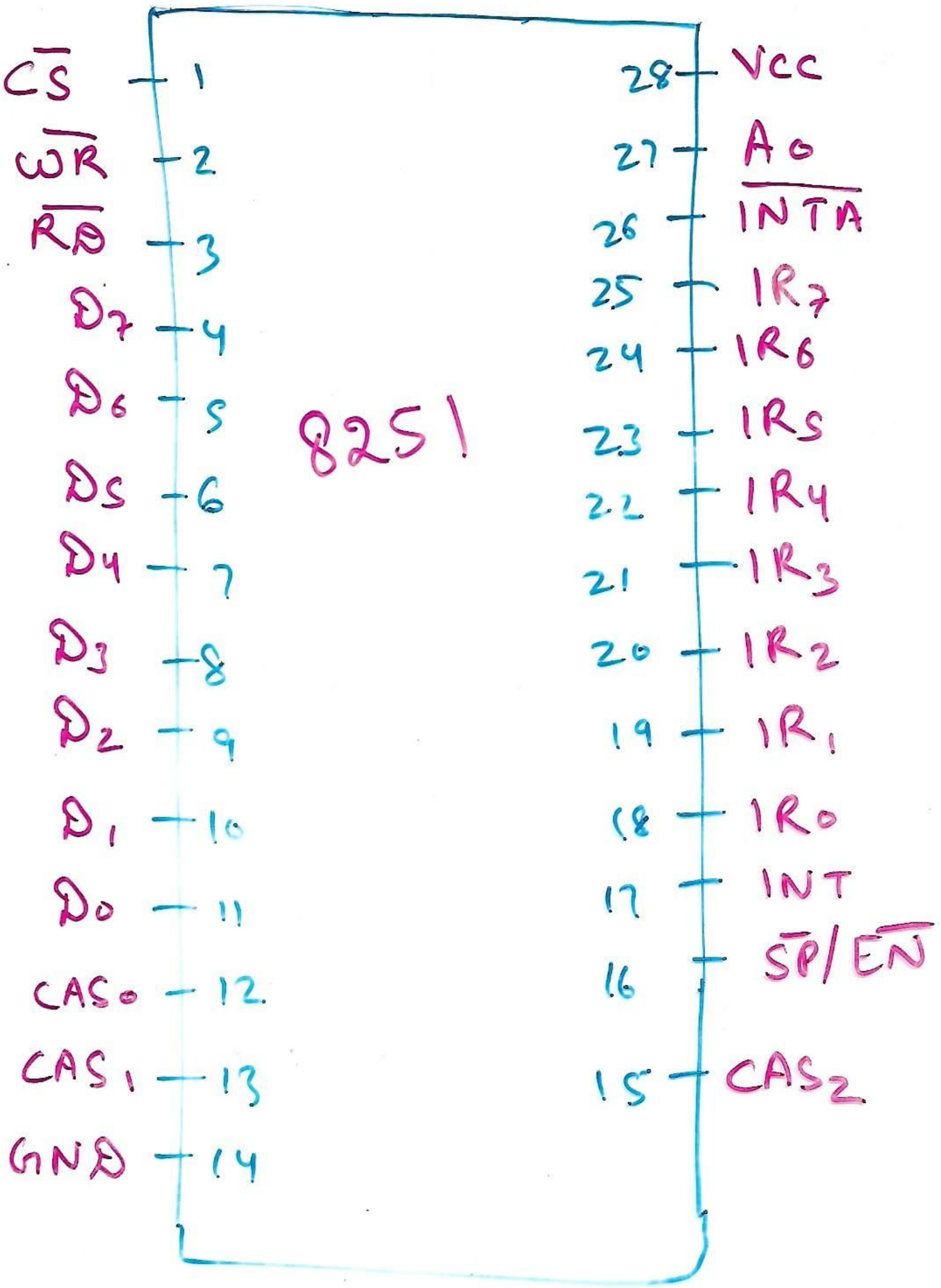
↳ Modes are indicated as :→

i/o without Handshaking **Mode 0**, **Mode 1**, **Mode 2** ↓ Bidirectional Handshake

Handshake strobed i/o operation



8259 Internal Block


8251
CS 1
WR 2
RD 3
D7 4
D6 5
D5 6
D4 7
D3 8
D2 9
D1 10
D0 11
CAS0 12
CAS1 13
GND 14
28 VCC
27 A0
26 INTA
25 IR7
24 IR6
23 IR5
22 IR4
21 IR3
20 IR2
19 IR1
18 IR0
17 INT
16 SP/EN
15 CAS2

Programming 8259 :-

a) Initialisation command words.
b) Operation Command words.
   1) Fully Nested Mode
   2) Rotating Priority Mode
   3) Special Mask Mode
   4) Polled Mode

→ Do Pin Diagram (Fig 8.14)

8251 :→ (Programmable Communication Interface)
(USART)

* Can be programmed in :-
   a) Synchronous mode
   b) Asynchronous mode

* Receives parallel data & transmits serial data or vice versa.

CS	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Operation
1	X	X	X	Data Bus 3-state
0	X	1	1	Do
0	1	0	1	status → CPU
0	1	1	0	Control word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU