Question Paper Solution

Q1= Attempt any ten Questions:

ⓐ Define instruction cycle?

Ans= The instruction cycle is the cycle that the central processing unit follow from boot-up until the computer has shut down in order to process instruction. It is composed of three main stage, the decode stage, and the execute stage. In simpler CPUs the instruction cycle is executed sequentially, each instruction being processed befor the next one is started.

ⓑ Explain Indexing?

Ans= Indexing means pointing or referencing objects with sequential number. In a library, book are arranged according to number. and they are referred to or sorted by number. This is called indexing.

ⓒ Define asynchroronous data transfer?

Ans= Asynchronous means 'at irregular intervals'. In this method data transfer is not based on prerdetermined timing pattern. This technique of data transfer is used when the speed of an I/o device is not predictable. the status of the I/O device i.e. whether the device is ready or not, is checked by the microprocessor before the data are transferred.

Asynchronous data transfer is used for slow I/O devices. The technique is an inefficient technique because the precious time of the microprocessor is wasted in waiting.

(d) What do you mean by intercept process?

Ans= The interrupt is a process of data transfer whereby an external device or a peripheral can inform the processor that it is ready for communication and it requests attention. The process is initiated by an external device and the response to an interrupt request is directed or controlled by the microprocessor.

(e) Differentiate between microprocessor and microcontroller?

Ans= # Microprocessor - • Microprocessor is off chip device. (RAM, ROM, I/O ports, CPU are connected externally).

- General Purpose Unit.
- High cost
- High power consumption.
- Used for high scale Application.

Microcontroller - • Microcontroller is on chip device. (RAM, ROM, I/O ports, CPU are connected internally)

- Specific purpose unit.
- Low cost

- Low power consumption
- Used for low scale Application.

(f) What is role of RS232C?

Ans= - It is the most widley used data Commication standerd for short distance & moderate data rate.

- It is used if data is transfered in the form of voltage signals

Features of RS 232C —

- Mode operation is signal ended.
- total number of drivers allowed to one line is 1 driver
- total number of receiver allowed to one line receiver.
- Maximum cable length 50 ft.
- Maximum date rate is 20 Kbps
- Maximum voltage supply is ± 25V.

(g) Define peripheral controlled data transfer?

Ans= Peripheral devices are those devices that are linked either internally or externally to a computer. These devices are commonly used to transfer data. The most common processes that are carried out in a computer are entering data and displaying processed data. Several devices can be used to receive data and display processed data The device used to perform these function are called peripherals or I/O devices.

The following are some of the commonly used pheripherals

- Keyboard- The Keyboard is the most commonly used input device. It is used to provide commands to the computer. The commands are usually in the form of text.

- Monitor- The most commonly used output device is the moniter. A cable connects the monitor to the video adapters in the computer's motherband. These video adaptors convert the electrical signals to the text and images that are displayed.

- Printer- Printers provide a permanent record of computer data or text on paper. We can classify printers as impact and non-impact printers.

(h) Define interrupt priority?

Ans= The 8085 microprocessor has five interrupt inputs... These interrupts have a fixed priority of interrupt service. If two or more interrupts service. If two or more interrupts go high at the same time, the 8085 will service them on priority basis. The TRAP has the highest priority followed by RST 7.5, RST 6.5, RST 5.5.

(i) Explain timing diagram?

Ans= To Know the working of 8085 microprocessor, we should know the timing diagram of 8085 microprocessor. With help of timing diagram, we can easily calculate the execution time of instruction and as well as program. Before going for timing diagram of 8085 microprocessor, we should know some diagram parameter to draw timing diagram of 8085 microprocessor. Those parameters are:

- Instruction Cycle • Machine cycle
- T-state

(J) Define PUSH and POP operation?

Ans=
- In case of PUSH operation, the SP register gets decreased by 2 and new data item used to insert on to the top of the stack.

- In case of POP operation, the data item will have to be deleted from the top of the stack and the SP register will get increased by the value of 2.

(K) Give example of bit address and byte address?

Ans=• Bit address.

(L) What do you mean by address and data buses?

Ans= A bus is a series of lines that connect the processor to another part of the computer's architecture, such as cache memory or main memory.

- Address Buses - The address bus is uni-directional. It is concerned with passing an address one way, from the CPU to RAM

- Data Buses - The data bus is bi-directional. It can carry data to main memory from the processor and vice versa. The data bus will transfer data to/from the address that is held on the address bus.

Date
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(m) What are SIM instructions?

Ans= In 8085 Instructions set, SIM stands for 'SetInterrupt Mask'. It is 1-Byte instruction and it is a multi-purpose instruction. The main uses of SIM instruction are—

- Masking /unmasking of RST7.5, RST6.5, and RST5.5
- Reset to 0 RST7.5 flip-flop
- Perform serial output of data

(n) List the role of supporting chips?

Ans= 'Chip' is short for microchip, the incredibly complex yet tiny modules that store computer memory or provide logic circuity for microprocessors. Perhaps the best Know chips are the Pentium microprocessors from intel. A chip is manufactured from a silicon. Chip is also sometimes called an IC or integrated circuit.

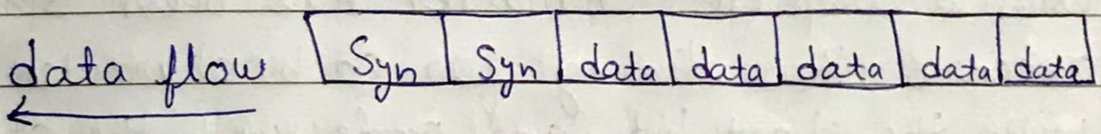
Q2= Attempt any 5 of the following questions:

(i) Explain in detail synchronous and asynchronous data transfer?

Ans= • Synchronous data transfer is a data transfer method in which a continuous stream of data signals is accompanied by timing signals to ensure that the transmitter and the receiver are in step with

one another. The data is sent in blocks spaced by fixed time intervals.
Synchronous transmission modes are used when large amounts of data must be transferred very quickly from one location to the other. The speed of the synchronous connection is attained by transferring data in large blocks instead of individual characters.
Synchronous transmission synchronizes transmission speeds at both the receiving and sending end of the transmission unsing clock signals built into each component. A continual stream of data is then sent between the two nodes.
The data blocks are grouped and spaced in regular intervals and are preceded by special character called syn of synchronous idle characters. See the fallowing illustration.

Fig: Synchronous transmission



The fallowing is a list of characteristics specific to synchronous communication:

- There are no gaps between characters being transmitted
- Timing is supplied by modems or other devices at each end of the connection.
- Special syn characters preceds the data being transmitted.
- The syn characters are used between blocks of data

for timing purposes.

- Asynchronous - The term asynchronous is used to describe the process where transmitted data is encoded with start and stop bits, specifying the begining and end of each character.

An example of synchronous transmission is shown in the following figure:

Fig2 Asynchronous transmission

Start-bit

Stop-bit

0	1	2	3	4	5	6	7	8	1

These additional bits provide the timing or synchronization for the connection by indicating when a complete character has been sent or received, thus, timing for each character begins with the start bit and ends with the stop bit.

When gaps appear between character transmission the asynchronous line is said to be in a mark state.

The following is a list of characheristics specific to asynchronous communication:

- Each character is preceded by a start bit and followed by one or more stop bits.

- Gaps or space between characters may exist.

With asynchronous transmission, a large text decoment is organised into long strings of latters that makes up the words within the sentences and paragraphs.

(ii) Explain the role of memory mapped I/O and I/O mapped I/O.

Ans= In memory mapping of I/O devices, the I/O ports are assigned 16-bit address within the memory. Here each bus is common thus the same set of instruction is used for memory and I/O devices. Thus I/O is considered as memory and the same address space is used by both memory and I/O devices. This reduces the addressing capability of the memory

In this case, the processor considers the I/O ports as memory locations for the purpose of reading and writing. So, whenever, an address is generated on the address bus then resultantly control signal is generated for momory read. In such a case, the processor is not concerned whether the responding data is coming from a memory device or an I/O device. The same is the case with the memory write operation.

I/O-mapped I/O

It is also know is Isolated I/O mapping and the reason for the same is that here the address space of memory and I/O are separated from each other. Thus, different read and write instruction are used for I/O and memory. In this approach, there is a common bus for I/O devices and memory however, individual read and write control lines are used for I/O. Here the operation takes place in a way that, if the data over which operation is to be performed is to be collected from the I/O devices then address is placed on the address line and I/O read and I/O write control lines will get activated so that data transfer can be performed between the processor and I/O.

For the transfer of data between the processor and I/O devices, only IN and OUT instructions are used in the isolated mapping. The required chip select signals in the case are generated by an individual decoding unit.

(iii) Define in brief the following ÷

① Logic instruction - Logical instruction of a microprocessor are simply the instruction that carry out basic logical operation such as OR, AND, XOR, and so on. In Intel's 8085 microprocessor, the destination operand for the instruction is always the accumulator register. Here, the logical operation work on a bitwise level. The corresponding result is also stored in the accumulator register.

② Brunch instruction- These instruction are very important because they allow the microprocessor to change the sequence of a program either conditionally or unconditionally. The conditional branch instruction transfer the program to the spencified level when certain condition is satisfied The unconditional branch instruction transfer the program to the specified location unconditionally

③ Machine control instruction- These type of instruction control machine function such as Halt, interrupt, or do nothing. This type of instruction alters the different type of operation executed in the processor.

- HLT- Halt and enter wait state. The contents of the registers are unaffected during the HLT state.

- NOP- No operation is performed. The instruction is fetched and decoded, however, no operation is executed.

- RIM- Read interrupt Mask. This is a multipurpose instruction used to read the status of interrupts 7.5, 6.5, 5.5 and to read serial data input bit.

- SIM - Set interrupt Mask. This is a multipurpose instruction and used to implement the 8085 interrupts and serial data output.

(iv) Explain the various addressing modes of 8085 microprocessor?

Ans= These are the instruction used to tranfer the data from one register to another register from the memory to the register, and from the register to the memory without any alteration in the content addressing modes in 8085 is classified into 5 groups —

- Immediate addressing mode-

In this mode, the 8/16-bit is specified in the instruction itself as one of its operand. For example: MVI K, 20F means 20F is copied into register K.

- Register addressing mode-

In this mode, the data is copied from one register to another. For example; MOV K, B; means data in register B is copied to register K.

- Direct addressing mode-

In this mode, the data is directly copied from the given address to the register. For example: LDB 5000k means the data at address 5000k is copied to register B.

- Indirect addressing mode-

In the mode, the data is transferred from one register to another by using the address pointed by the register. For example: MOV K, B: means data is transferred from the memory address pointed by the register to the register K.

- Implied addressing mode-

This mode doesn't require any operand, the data is specified by the opcoder itself. For example: CMP

(v) Explain 8255 programmable peripheral interface in detail.

Ans= The 8255 A is a general purpose programmable I/O device designed to transfer the data from I/O to interrupt I/O under certain conditions as required. It can be used with almost any microprocessor.

It consists of three 8-bit bidirectional I/O ports (24 I/O lines) which can be configured as per the requirement.

PORTS OF 8255A

8255A has three ports i.e, PORT A, PORT B, and PORT C.

- Port A contains one 8-bit output latch/buffer and one 8-bit input buffer.

- Port B is similar to PORT A.
- Port C can be split into two parts, i.e. PORT C lower and PORT C upper by the control word.

These three ports are futher divided into two groups i.e Group A includes PORT A and upper PORT C Group B includes PORT C. These two groups can be programmed in three different modes, i.e, the first mode is named as mode 0, the second mode is named as Mode 1 and the third mode is named as Mode 1 and the third mode is named as Mode 2.

Operating Modes-

8255A has three different operating modes:—

- Mode 0 – In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports. Each port can be programmed in either input mode or output mode where output are latched and inputs are not latched.

- Mode 1- In this mode, Port A and B is used as 8-bit I/O ports. They can be configured as either input or output ports. Each port uses three lines from port C as hand shake. inputs and outputs are latched.

- Mode 2- In this mode, Port A can be configured as the bidirectional port and port B either in Mode 0 or Mode 1 Port A uses five signals from Port C as hand shake Signals for data transfer.

Features of 8255A

The prominent feature of 8255A are as follows-

- It consists of 3-8 bit IO ports i.e. PA, PB and PC.

- Address/data bus must be externally demux'd
- It is TTL compatible.
- It has improved DC driving capability.

(vi) Discuss arithmetic operation of 8085 microprocessor?

(vii) Mention the function of MEMR & MEMW in 8085?

Ans=

(viii) Define address bus and data bus?

Address Bus—

Ans= In Computer Architecture, a Bus is defined as a system that transfer data between hardware components of a computer or two separate computer It is a set of parallel wires connecting two or more components.

The Address Bus will carry the data that spacifies the address of a memory location, to either write to that location, or to read from that location.

Notice that there is a one-way connection from the processor to the address bus and a one-way connection from the address but to the main memory, or the I/O devices. The address bus is a one direction bus, which allows the processor (CPU) to get access to addressable units such as a memory location, or an I/O controller or device.

The address bus is UNI-directional which is one way. Where as OMNI-directional is all directions, which the address bus is not! Sorry about that!. The processor is a 6502 with a 16 bit address bus, allowing for a 64 kilobytes of memory. You will see that the processor has 16 address lines A0-A15, giving 65,536 memory location. The address bus has a role in the retrieval of data from a memory location by the CPU. The CPU will sand the address of the memory location of the data required on the address bus. The data in the memory location will then be sent back via the data bus and will be received by the CPU in processing.

Data Bus- Data Bus also called electronic databus any collection of data, or information, that is specially organized for rapid search and retrievel by a computer. Databuses are structured to facilitate the storage, retrievel, modification, and deletion of data in conjuction with various data-processing operations.

A Data Bus is stored as a file or a set of files. The information in these files may be broken down into records, each of which consist of one or more fields. Fields are the basic units of data storage and each field typically contains information pertaining to one aspect or attribute of the entity described by the database. Records are also organized into tables that include information about relationship between its various fields. Although data bus is applied loosely to any collection of information in computer files, a database in the Strict sense provides cross-referencing capabilities. Using Keywords and various sorting commands, users can rapidly search, rearrange, group, and select the fields in many records to retrieve or create reports on particular aggregates of data. Data bus records and files must be organised to allows retrievel of the information.

Part-B

Q3=

(a) Explain conditional and return instruction in microprocessor programming.

Ans= # Conditional Branch Instructions - On the other hand, conditional branches are those instruction whose execution is based on some condition. It checks one or more flag conditions and transfer the control to a new memory location. There are two type of jumps namely far and Near. In the far jumps, the program counter jumps to the memory location which lies outsides the current code segment whereas in near jumps, the IP points to the memory address inside the current code segment and that is why the CS register remains unchanged in near jumps. The conditional jumps are also near jumps. ~~The syntax of these instructions is~~

Return Instruction - The program sequence is transferred from the subroutine to the calling program based on the specified flag of the PSW as described below. The two bytes from the top of the ~~sg~~ stack are copied into the program counter, and program execution begins at the new address.

- RC- The program sequence is transferred to a particular level or a 16-bit address if C=1 (or carry is 1).

  Eg- RC ABC (jump to the level abc if C=1)

- RNC - The program sequence is transferred to a perticular level or a 16-bit address if C=0 (or carry is 0)

  Eg- RNC ABC (jump to the level abc if C=0)

- RP- The program sequence is transferred to a particular level or a 16-bit address if S=0 (or sign is 0).

  Eg- RP ABC (jump to the level abc if S=0)

- RM - The program sequence is transferred to a particular level or a 16-bit address if S=1 (or Sign is 1)

  Eg -RM ABC (jump to the level abc if S=1)

- RZ - The program sequence is transferred to a particular level or a 16-bit address if Z=1 (or zero flag is 1)

  Eg- RZ ABC (jump to the level abc if Z=1)

- RNZ- The program sequence is transferred to a particular level or a 16-bit address if Z=0 (or zero flag is 0)

  Eg- RNZ ABC (jump to the level abc if Z=0)

- RPE- The program sequence is transferred to a particular level or a 16-bit address if P=1 (or parity is 1)

  Eg- RPE ABC (jump to the level abc if P=1)

- RPO- The program sequence is transferred to a particular level or a 16-bit address if P=0 (or parity is 0)

  Eg- RPO ABC (jump to the level abc if P=0

- RET- Return from subroutine unconditionally

(b) Draw and explain the timing diagram for read and write operation.

Ans= These are explained in steps-

- When processor is ready to initiate the bus cycle, It applies a pulse to ALE during T1. Before the faling edge of ALE, the address. BHE. M/IO, DNE and DT/R must be stable i.e DEN = high and

DT/R = 0 for input or DT/R = 1 for output.

- At the trailing edge of ALE, ICs 74LS373 or 8282 latches the address.

- During T2 the address signals are disable and S3-S7 ale available on AD16/S3-AD19/S6 and BHE/S7. Also DEN is lowered to enable transeiver.

- In case of input operation, RD is activated during T2 and AD0 to AD15 go in high impedance preparing for input.

- If memory or I/O interface can perform the transfer immediately, there are no wait states and data is output on the bus during T3.

- After the data is accepted by the processor RD is raised high at the beginning of T4.

- Upon detecting this transition during T4, the memory or I/O device will disable its data signals.

- For an output operation, processor applies WR = 0 and then the data on the data bus during T2.

- In T4, WR is raised high and data Signals are disabled.

Q4= Write short on the following-

(i) DMA controller- DMA controller is a hardware device that allows I/O devices to directly access memory with less participation of the processor. DMA controller needs the same old circuits of an interface to communicate with the CPU and Input/output divices.

DMA Controller has three registers as follows:

- Address register- It contains the address to spacify the desired location in memory.
- Word Count register- It contains the number of words to be transferred.
- Control register- It specifies the transfer mode.

Operation of DMA Controller in Microprocessor-

Basically whenever an I/O device needs to transfer the data to the memory, then it initially sends a request to DMA controller. On receiving data transfer request the controller sends HOLD request to the CPU and waits for HLDS which is nothing but hold acknowledge by the CPU

So, on getting HOLD request by the controller, the CPU leaves the control over all the buses and sends HLDS to the controller.

(ii) Interrupt driven data transfer :-

- The interrupt driven data transfer scheme is the best method of data transfer for effectively utilizing the processor time.

- In this scheme, the processor first initiates the I/o device for data transfer.

- After initiating the device, the processor will contine the execution of instructions in the program.

- Also at the end of an instruction the processor will check for a valid interrupt signal.

- If there is no interrupt then the processor will continue the execution

- When the I/O device is ready, it will interrupt the processor.

- On receiving an interrupt then the processor will complete the current instruction execution and save the processor status in stack.

- Then the processor calls an interrupt Service routine (ISR) to service the interrupted device.

- At the end of ISR the processor status is retrieved from stack and the processor starts executing its main program.

(iii) Stack and its function—

A stack is a linear data sturture that follows the LIFO principle. Stack has one end, whereas the Queue has two ends. It contains only one pointer top pointer pointing to the topmost element of the stack. Whenever an element is added in the stack, it is added on the top of the stack, and the element can be deleted only from the stack. In other words, a stack can be defined as a container in which insertion and deletion can be done from the one end known as the top of the stack.

Some common operations implemented on the stack

- Push (): When we insert an element in a stack then the operation is know as a push.

- POP(): When we delete an element from the stack, the operation is know as a pop.

- is Empty(): It determines whether the stack is empty or not.

- is Full(): It determines whether the stack is full or not.

- Peek(): It returns the element at the given position.

- Count(): It returns the total number of elements available in a stack.

- Change(): It change the element at the given position.

- Display(): It prints all the element available in the stack.

(iv) Arithmetic instruction–

Arithmetic instruction are the instructions which perform basic arithmetic operations such as addition, subtraction and a few more. In 8085 microprocessor the destination operand is generally the accumulator. In 8085 microprocessor, the destination operand is generally the accumulator. The arithmetic instruction are further classified into binary, decimal, logical, shift/rotate, and bit/byte manipulation instructions.

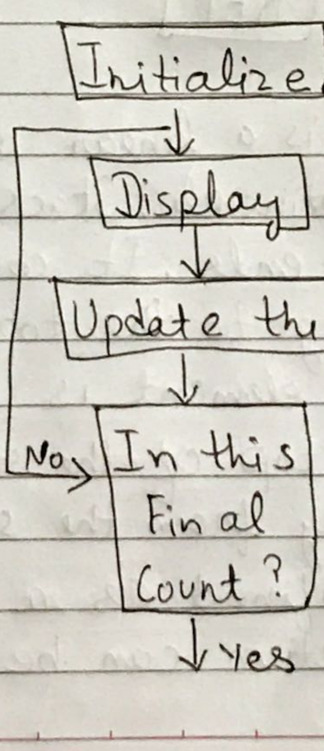
Type of arithmetic instructions-

- Addition
- Subtraction
- Multiplication
- Division

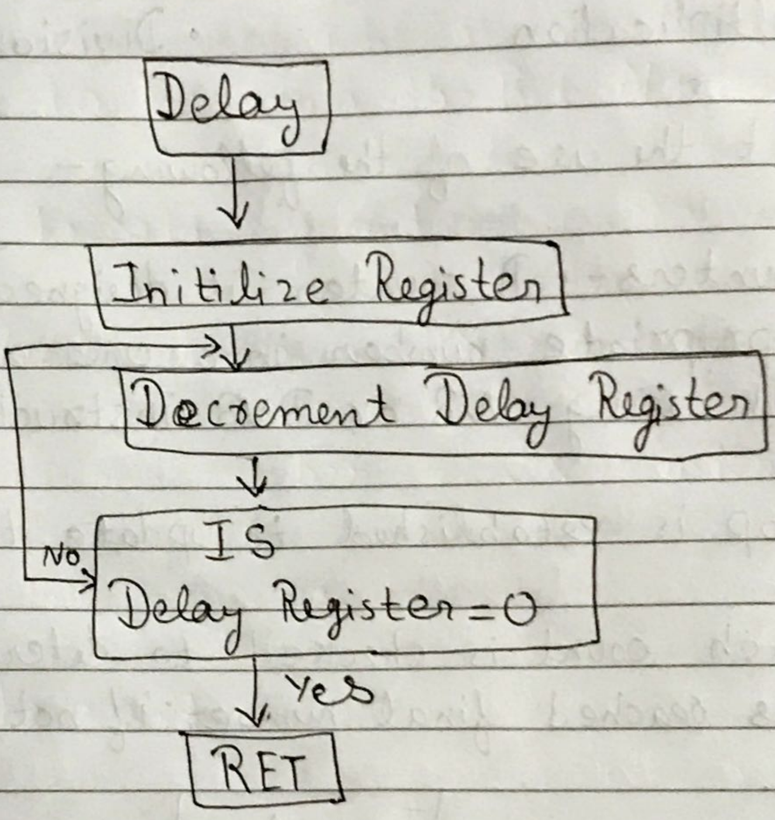
Q6= List the use of the following-

(i) Counters- • A counter is designed simply by loading appropriate number into one of the registers and using INR or DNR instructions.

- Loop is established to update the count.
- Each count is checked to determine whether it has reached final number: if not, the loop is repeated.



(ii) Time delays- Procedure used to design a specific delay. A register is loaded with a number, depending on the time delay required and then the register is decremented until it reaches zero by setting up a loop with conditional jump instruction.



(iii) Stacks- A stack is a linear data structure that follows the LIFO principle. Stack has one end, whereas the Queue has two ends. It contains only one pointer top pointer pointing to the topmost element of the stack. Whenever an element is added in the stack, it is added on the top of the stack, and the element can be deleted only from the stack. In other words a stack can be defined as a container in which insertion and delection can be done from the one end know as the top of the stack.

(iv) Routines - A routine or subroutine, also referred to as a function, procedure, method and subprogram, is called and executed anywhere in a program. For example, a routine may be used to save a file or display the time. Instead of writing the code each time these commonly performed tasks are needed, routines are created and called when these tasks needs to be performed.

Q7= (a) Write a program for the additions of two 16-digit numbers.

Ans= Program should use registers AX and BX to ~~that~~ take first and second number to find the sum of two numbers.

Consider that a word of data is present in the AX register and a 2nd word of data is present in the BX register.

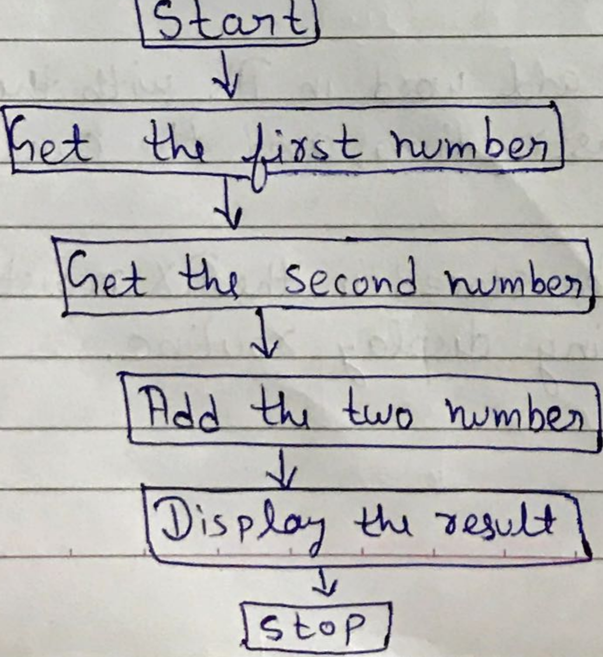
We have to add word in AX with the word in BX. Using ADD instruction, and the contents.

Result will be stored in the AX register. Display the result using display routine.

For example:	
AX = 1234 H	1234 H
BX = 0100H	0100 H
	1334 H

Algorithm to Add two 16-Bit Numbers

- Initialize the data segment.
- Get the first number in AX register.
- Get the second number in BX register.
- Add the two numbers.
- Display the result
- Stop



Program to Add two 16 Bit Numbers:

We are taking two numbers as input using AX and BX registers which we will be using to calculate sum. After calcalating sum we have to print the result as show in below code. Please find the steps which are required to run this program at the end. You should have TASM installed on your machine so that you can run this code.

(b) Explain in detail about machine cycle of 8085.

Ans= The machine cycle is the most basic operation that a computer performs, and in order to complete menial tasks such as showing a single character on the screen, the CPU has to perform multiple cycles. The computer does this from the mement it boots up until it shuts down.

The steps of a machine cycle are:

- Fetch - The control unit requests instructions from the main memory that is stored at a memory's location as indicated by the program counter (also known as the instruction counter).

- Decode - Received instructions are decoded in the instruction register. This involves breaking the operand field into its components based on the instruction's operation code (opcode)

- Execute - The involves the instruction's op code as it specifies the CPU operation required. The program counter indicates the instruction sequence for computer. These instructions are arranged into the instruction register and as each are executed, it increments the program counter so that the next instruction is stored in memory. Appropriate circuitry is then activated to perform the requested task. As soon as instructions have been executed, it restarts the machine cycle that begins the fetch step.